ABSTRACT OF THE DISCLOSURE

A memory module has a plurality of DRAMs (115), which share a bus line, on the front surface and the back surface of a board. The bus line is connected through a via hole (113) from a terminal (111) to one end of a strip line (112), and the other end of the strip line is connected to a strip line in the other layer through a via hole (119) provided for looping back the line. A termination resistor (120), provided near a termination voltage terminal (VTT), is connected to the looped-back strip line in the other layer through a via hole. The DRAM terminals are connected to the strip line each through a via hole. This memory module is mounted on a motherboard, on which a memory controller is provided, through a connector. The effective characteristic impedance of the bus line is matched with the characteristic impedance of the line in the motherboard.